Program : **Diploma in Electronics Engineering**	
Course Code : **6041B**	Course Title: **Verilog HDL and Programmable Logic Devices**
Semester : **6**	Credits: **4**
Course Category: **Program Elective**	
Periods per week: **4 (L:4, T:0, P:0)**	Periods per semester: **60**

Course Objectives:

- To provide awareness on the basics of Hardware Description Language,
- Programmable Logic Devices and its use in designing Digital Electronics Circuits.

Course Prerequisites:

Topic	Course Code	Course Title	Semester
Electronics Components and Circuits	3043	Electronic Circuits	3
Combinational and Sequential digital circuits	3044	Digital Electronics	3
Basics concepts of programming	3045	Fundamentals of C Programming	3

Course Outcomes:

On completion of the course, the student will be able to,

COn	Description	Duration (Hours)	Cognitive level
CO1	Outline the basics of Hardware Description Language and program structure	14	Understanding
CO2	Make use of gate level modelling and dataflow modelling to design digital circuits	15	Applying
CO3	Make use of Behavioural Modelling to design combinational and sequential circuits	15	Applying
CO4	Outline the architecture of CPLDs and FPGA	14	Understanding
	Series Test	2	

CO -PO Mapping:

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7
CO1	2						
CO2	3		2				
CO3	3		2				
CO4	2						

3-Strongly mapped, 2-Moderately mapped, 1-Weakly mapped

Course Outline:

Module Outcomes	Description	Duration (Hours)	Cognitive Level
CO1	**Outline the basics of Hardware Description Language and program structure**		
M1.01	Explain the evolution of Computer Aided Design, HDL, and importance of HDL	3	Understanding
M1.02	Explain hierarchical modelling concepts	4	Understanding
M1.03	Explain Design block – stimulus-data types	4	Understanding
M1.04	Explain the concept of Verilog Modules and Ports	3	Understanding

Contents:

Evolution of Computer Aided design, Overview of Digital design with Verilog HDL - Evolution of CAD - emergence of HDLs, typical HDL based design flow- why Verilog, trends in HDLs. Hierarchical Modelling Concepts - Top-down and bottom-up design methodology, differences between modules and module instances, components of a simulation. Design block, stimulus block, basic concepts, Lexical conventions, data types, system tasks, compiler directives.

Module - Components of a Verilog module, Ports - definition, list of ports, port declaration, port connection rules

CO2	**Make use of gate level modelling and dataflow modelling to design digital circuits**		
M2.01	Identify logic gates as predefined primitives	1	Understanding
M2.02	Illustrate the instantiation of basic gates	1	Understanding
M2.03	Make use of gate level modelling to design different Combinational logic circuits	3	Applying
M2.04	Describe gate delays, minimum value, typical value and maximum value.	1	Understanding

M2.05	Describe continuous assignment statement and implicit continuous assignment statement	1	Understanding
M2.06	Explain regular assignment delay, implicit continuous assignment delay and net declaration delay	1	Understanding
M 2.07	Describe the basis of dataflow modelling, expressions operators and operands	3	Understanding
M 2.08	Make use of dataflow modelling to design combinational and sequential logic circuits	4	Applying
	Series Test 1	1	

Contents:

Gate level modelling - Instantiation of basic gates, design of simple combinational circuits using gate level modelling life multiplexer, full adder and ripple carry adder, gate delays, gate delays, minimum value, typical value and maximum value

Data flow modelling - continuous assignment statement , implicit continuous assignment statement, regular assignment delay, implicit continuous assignment delay and net declaration delay, expressions operators and operands, different types of operators, design of simple combinational and sequential circuits - full adder, multiplexer, d flip flop, ripple counter

CO3	**Make use of Behavioural Modelling to design combinational and sequential circuits**		
M3.01	Explain the significance of structured procedures always and initial in behavioural modelling	3	Understanding
M3.02	Explain procedural assignments.	3	Understanding
M3.03	Identify conditional statements used in behavioural modelling	3	Applying
M3.04	Identify the looping statements used in Verilog,	3	Applying
M3.05	Develop Verilog programs to realize simple combinational and sequential circuits using behavioural modelling	3	Applying

Contents:

Behavioural Modelling -Structured procedures, initial and always, blocking and non-blocking statements - explanation with examples. Delay control, event control, conditional statements, looping statements, simple design examples (4-1 Multiplexer, 4-bit counter etc..)

CO4	**Outline the architecture of CPLDs and FPGA**		
M4.01	Explain the architecture of PAL and PLA	4	Understanding
M4.02	Explain CPLD with the help of block schematic	3	Understanding

M4.03	Illustrate the architecture of FPGA	4	Understanding
M4.04	Explain configurable logic blocks (CLBs)	1	Understanding
M4.05	Compare FPGA with CPLD	2	Understanding
Test 2		1	

Contents:

Simple Programmable Logic Devices, Architecture of PAL and PAL ,compare PAL and PLA, Complex Programmable Logic Devices - Architecture and applications, Field Programmable Gate arrays - Architecture and applications, comparison of CPLD and FPGA, Concept of configurable logic blocks

Text / Reference Books:

T/R	Book Title/ Author
T1	Verilog HDL –Samir Palnitkar-Pearson Education
T2	Digital design Morris mano, Third Edition, PHI
R1	Digital Design	With an Introduction to the Verilog HDL, VHDL, and SystemVerilog	Sixth Edition	By Pearson Paperback –2018 by M. Morris Mano , Michael D.Ciletti
R2	FPGA based system design Wayne Wolf, Pearson Education
R3	T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
R4	FPGA protyping by Verilog examples –PONG P Chu - Willey
R5	HDL Prgramming- Nazeih M Botros- Dream Tech
R6	Digital Systems Design with FPGAs and CPLDs -Ian Grout, Elsevier

Online Resources:

Sl.No	Website Link
1	https:/nptel.ac.in/courses/106/105/106105165/
2	https://www.tutorialspoint.com/vlsi_design/vlsi_design_verilog_introduction.htm
3	http://www.ee.ic.ac.uk/pcheung/teaching/ee2_digital/fpga%20&%20cpld%20tutorial.pdf
4	https://www.youtube.com/watch?v=PJGvZSlsLKs
5	https://www.youtube.com/watch?v=pR6-aNxHNac